CLAIMS

1. A device comprising:

a spin-dependent tunneling cell including first and second ferromagnetic elements separated by a tunnel barrier layer, said first ferromagnetic element having a first magnetic moment and said second ferromagnetic element having a second magnetic moment;

a first electrically conductive line that is disposed adjacent to one of said ferromagnetic elements and provides a magnetic field that changes a direction of said first magnetic moment relative to that of said second magnetic moment; and

a second electrically conductive line that is electrically connected to at least one of said ferromagnetic elements to sense whether electrons can tunnel across said barrier layer, said second electrically conductive line being connected to a plurality of transistors in parallel.

2. The device of claim 1, wherein said first electrically conductive line is electrically connected to at least one of said ferromagnetic elements.

3. The device of claim 1, wherein said transistors share a source region.

4. The device of claim 1, wherein said read line includes an uninterrupted electrically conductive path between each of said transistors and said one of the ferromagnetic elements to which said read line is connected.

5. The device of claim 1, wherein said transistors are field effect transistors.

6. The device of claim 1, wherein said transistors are CMOS transistors.

7. The device of claim 1, wherein at least one of said ferromagnetic elements includes a half-metallic magnet.

8. The device of claim 1, further comprising a pinning structure coupled to said second ferromagnetic element to hold said second magnetic moment in a first direction.

9. The device of claim 1, further comprising a plurality of spin-tunneling cells connected to said first electrically conductive line.

10. A device comprising:

a plurality of spin-dependent tunneling cells each of which has a state that is one of a plurality of states;

first and second electrically conductive lines that are disposed adjacent to one of said cells to change said state from a first state to a second state; and

a third electrically conductive line that is electrically connected to said one cell to read said states, said third electrically conductive line being connected to a plurality of transistors in parallel.

11. The device of claim 10, wherein said first electrically conductive line is electrically connected to said one cell.

12. The device of claim 10, wherein said transistors share a source region.

13. The device of claim 10, wherein said read line includes an uninterrupted electrically conductive path between each of said transistors and said one cell.

14. The device of claim 10, wherein said transistors are field effect transistors.

15. The device of claim 10, wherein said transistors are CMOS transistors.

16. The device of claim 10, wherein each of said cells includes a ferromagnetic layer.

17. The device of claim 10, wherein each of said cells includes a half-metallic magnetic layer.

18. The device of claim 10, wherein said first electrically conductive line is disposed adjacent to a set of said cells.

19. The device of claim 10, wherein said transistors are each connected to ground.

20. A device comprising:

a plurality of spin-dependent tunneling cells each of which has a state that is one of a plurality of states;

an electrically conductive bit line that is electrically connected to at least one of said cells;

an electrically conductive digit line that is disposed adjacent to said one cell, such that electrical current flowing simultaneously in said bit line and said digit line changes said state of said one cell from a first state to a second state; and

an electrically conductive read line that is electrically connected to said one cell and connected to a plurality of transistors in parallel, to read said state of said one cell when said transistors are all turned on.

21. The device of claim 20, wherein said transistors are each controlled by a word line.

22. The device of claim 20, wherein said transistors share a source region.

23. The device of claim 20, wherein said bit line extends in a first direction and said digit line extends in a second direction, said first and second directions being substantially perpendicular to each other.

24. The device of claim 20, wherein said transistors are field effect transistors.

25. The device of claim 20, wherein said transistors are CMOS transistors.

26. The device of claim 20, wherein each of said cells includes a ferromagnetic layer.

27. The device of claim 20, wherein each of said cells includes a half-metallic magnetic layer.